REMARKS

I. Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a), asserting that the drawings failed to show features as described in the specification. The Examiner cited, as an example, FIG. 1, indicating that the gate oxide is not shown. In FIG. 2, the Examiner argued that LDD is not shown. The Examiner therefore requested that the Applicant revise all figures without adding any new material. In response to the Examiner's request to revise the Figures, Applicant has amended the specification as indicated herein so that it is not necessary to revise the figures. For example, the detailed description section of Applicant's specification as now amended no longer indicates with respect to FIG. 1, the term "gate oxide".

Thus, the Applicant submits that it is no longer necessary to revise FIG. 1. Similarly, the detailed description section as amended with respect to the FIG. 2 descriptive text, indicates that LDD is shown through the introduction of resists 20-32, which assist in forming a drain. Accordingly, the Applicant submits that the objection to the drawings has now been traversed.

II. Specification

The Examiner stated that 35 U.S.C. 112, first paragraph, requires that the specification be written in "full, clear, concise and exact terms." The Examiner argued that the specification includes terms, which are not clear, concise and exact. The Examiner indicated that the specification should be revised in order to comply with 35 U.S.C. 112.

The Examiner cited, as examples, of such non-compliance under 35 U.S.C. 112, first, paragraph, the following:

On page 12, paragraph 38, the Examiner indicated that salicide gate is disclosed without steps for the formation of the salicide gate. The Examiner indicated that the specification stated that "SAC may be configured for use with the semiconductor step" without steps for forming or description as to how the SAC may be configured. The Applicant respectfully disagrees with this assessment. The statement "SAC may be configured for use with the semiconductor step" satisfies the formation of the salicide gate. The phrase "configured" in and of itself is a formation or creation step. When an item or thing is "configured," it is formed or created. The Applicant submits that one skilled in the art would have sufficient enablement and teaching via the phrase "SAC may be configured for use with the semiconductor step" in order to form a salicide gate thereof.

The Examiner further indicated that "Combining, the self-aligned contact and the salicide gate in the same cell area can effectively reduce gate resistance" is recited without any description of the method as to how the combination is achieved. The Applicant respectfully disagrees with this assessment. The sentence "Combining, the self-aligned contact and the salicide gate in the same area" in and of itself is sufficient to enable one skilled in the art to practice that particular step. The self-aligned contact and salicide gate can be combined in the same cell area to reduce gate resistance. The Applicant believes that it is not necessary to provide any further description of such a combining step, because that particular statement is sufficient in and of itself to enable one skilled in the art to understand clearly and concisely what must happen, i.e., the self-aligned contact and salicide gate can be combined in the same cell area.

The Examiner argued that on page 14, paragraph 40, the recitation that a "poly gate is defined" does not describe how the gate is defined and does not point out the gate. The Applicant respectfully disagrees with this assessment. The term "defined" does not mean that the poly gate is actually formed, only that the poly gate is being "set up" or defined for the formation. The poly gate is formed to

include poly plugs 34, 36 and 38. Although the poly gate may not actually be shown in a particular step, it is important to realize, as indicated in the specification, that "in FIGS. 1 to 15 herein, analogous parts are indicated by identical reference numerals" and that "FIGS. 1 to 15 together represent a semiconductor fabrication process that may be implemented in accordance with a preferred or alternative embodiments of the present invention." Thus, for example, with reference to all of the Applicant's figures in their entirety, one skilled in the art would recognize the formation and/or definition of a poly gate or other features and thus it is not necessary to point out the poly gate because the figures in and of themselves. For example, a poly gate should include poly plugs 34, 36, and 38, which are shown in the various figures.

The Examiner argued that on page 14, paragraph 41, it is stated that "third step 14 illustrates plug implant" and that there is not a description of a plug implant and no indication of a plug implant in the figure. The Applicant respectfully disagrees with this assessment. FIG. 3 of Applicant's specification shows poly plugs 34, 36, and 38 which are plug implants. Thus, a description of a plug implant is shown in the specification and one or more of the figures, which as indicated above, are to be interpreted together in their entirety, rather than as individual distinct inventions.

The Examiner argued that on page 15, paragraph 43, the recitation "involves an oxide/silicon nitride etch back step" does not explain how an oxide/silicon nitride etch back step is involved in the process. The Applicant respectfully disagrees with this assessment. An "etch back step" is a standard step in semiconductor processes. Thus, the use of the term oxide/silicon nitride etch back step is sufficient in and of itself as a clear and concise description of a desired step to be performed as part of the inventive process described in the specification.

The Examiner additionally argued that on page 15, paragraph 43, "LDD implant 50 layer is deposited" is not clear how implantation and deposition can be done and appears to be contradictory. The Applicant respectfully disagrees wit h this assessment. The term "deposited" refers to a "deposition" step. It is not necessary to explain in further detail how a deposition can be performed, because the term deposition or deposited is a well known term to those skilled in the art. Thus, the Applicant submits that the phrase "LDD implant 50 layer is deposited" is sufficient, because it is a clear and concise explanation and the term "deposited" speaks for itself. Additionally, the Examiner has not explained how the use of "LDD implant layer" is contradictory, and if so, why this does or does not enable the claims and adds or subtracts from the inventive processes disclosed in Applicant's claims and specification.

Different language

The Examiner further stated that the specification is replete with undefined acronyms like "RPO" on page 17 and requested appropriate corrections. The Applicants respectfully disagree with this assessment. The Applicant has amended the specification as indicated herein to remove the term "RPO." In addition, the Applicant points out that many of the acronyms are adequately defined in the specification. For example, LDD is defined as "lightly doped drain," TEOS is defined as Tetraethoxysilane, and so forth.

gate oxide

III. Title of the Invention

Regarding the title of the invention, the Examiner asserted that the title is not descriptive. The Examiner stated that a new title is required that is clearly indicative of the invention to which the claims are directed. The Applicant therefore requests that the following new title replace the old title: "Methods and Systems for Forming Embedded DRAM for an MIM Capacitor". If this new title does not appear descriptive enough to the Examiner, the Applicant invites the Examiner to suggest a new title.

IV. Rejections Under 35 U.S.C. § 112

The Examiner rejected claims 1-28 under 35 U.S.C. § 112, first paragraph, as containing matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to maker and/or use the invention.

Regarding claims 1 and 14, the Examiner argued that the method of forming an MIM capacitor and a self aligned contact is not described in the specification in such a way as to enable a person skilled in the art to make and/or use the invention. The Applicant respectfully disagrees with this assessment. The Applicant submits that the inventive steps disclosed in Applicant's specification, including claims 1 to 14, provide in their totality, a thorough description of a method for forming an MIM capacitor and a self-aligned contact in such a manner as to enable a person of ordinary skill in the art to make and/or use the invention. The Examiner has not explained how the method of forming an MIM capacitor and a self-aligned contact as disclosed in claims 1 to 14 is not described in the specification in such a way as to enable a person skilled in the art to make and/or use the invention. The Applicant therefore requests that the rejection to claims 1 to 14 under 35 U.S.C. 112, first, paragraph, be withdrawn.

Regarding claims 15 and 28, the Examiner argued that the system for fabricating an MIM capacitor and self aligned contact is not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Applicant respectfully disagree with this assessment. The Applicant submits that the argument presented above with respect to claims 1 to 14 applies equally to the rejection to claims 15 and 28 and 14-28 under 35 U.S.C 112. The Applicant therefore requests that the rejection to claims 15 and 28 and under 35 U.S.C. 112, first paragraph, be withdrawn.

V. Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Huang et al., (U.S. Patent No. 6,146,941) in view of S. Wolf (Silicon Proceeding for the VLSI Era, Vol. 2, Pages 144-152).

Regarding claim 1, the Examiner argued that Huang discloses in columns 4-6, and in Figures 2A-2F, a method of fabricating a capacitor formed on a substrate wherein the capacitor is used in a semiconductor device comprising the following steps: designating a gate comprising polysilicon (206) for the semiconductor device; configuring a self aligned contact, in column 5 and lines 27-28, for the semiconductor device and; combining the gate and SAC in a memory cell area of the semiconductor device, in column 4, and lines 65-66. The Applicant respectfully disagrees with this assessment. Column 5, lines 27-28 does not show a step of configuring a self-aligned contact. Instead, column 5, lines 27-28 refers to a contact window 111 as shown in FIG. 1H of Huang et al. A contact window 111 is not a "contact" as taught by Applicants' invention. Additionally, column 5, lines 27-28 does not teach any "self aligning" features. The Examiner has not explained how such self aligning features are taught or disclosed by Huang et al.

Additionally, Huang et al does not teach combining a gate and SAC in a memory cell area of the semiconductor area. Column 4 and lines 65-66 disclose instead simply a source/drain region 210 and a commonly used source/drain region 210a along with the location of gates 202 under a substrate surface 201. The material cited by the Examiner does not teach that an SAC and a gate can be combined in a memory cell area. Additionally, these citations of Huang et al do not indicate that the combining a salicide gate (Huang does not teach a salicide gate) and a self-aligned area in a memory cell area can permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance.

In fact, the Examiner admitted that Huang et al lacks a salicide gate. The Examiner argued, however, that Wolf teaches in Figures 3-39 on page 145 salicide gate processing steps along with SAC. The Examiner therefore argued that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Huang et al with that of Wolf to fabricate a capacitor in a semiconductor device with a low contact resistance and to increase memory cell density. The Applicant respectfully disagrees with this assessment because the Examiner has not provided a motivation for combining Figures 3-39 on page 145 with features of Huang (which, as explained above, do not teach the elements of Applicant's claim 1) to derive Applicant's invention.

The Applicants remind the Examiner that the references may not be taken out of context and combined without motivation, in effect producing the words of the claims (and sometimes, not even the words or concepts of the claims), without their meaning or context. The resultant combination would not yield the invention as claimed. The claims are rejected under 35 U.S.C. 103 and no showing has been made to provide the motivation as to why one of skill in the art would be motivated to make such a combination, and further fails to provide the teachings necessary to fill the gaps in these references in order to yield the invention as claimed.

The rejection under 35 U.S.C. 103 has provided no more motivation than simply to point out the individual words of the Applicants' claims among the references, but without the reason and result as provided in the Applicants' claims and specification, and without reason as to why and how the references could provide the Applicants' invention as claimed. Hindsight cannot be the basis for motivation, which is not sufficient to meet the burden of sustaining a 35 U.S.C. 103 rejection.

Regarding claims 2-13, the Examiner rejected claims 2-13 as dependent upon claim 1. Regarding claims 14-28, the Examiner rejected claims 14-28 under

35 U.S.C. 112, first paragraph. The Applicant submits that the arguments presented above against the rejection to claim 1 under 35 U.S.C. 103 also apply equally to the rejection to claims 2-13.

Thus, claims 1-28 of the present invention are not taught or suggested by Huang et al or Wolf, alone or in combination with one another. Combining these references fails to teach or yield the invention as claimed. The combination of these references fails to teach or suggest all the elements of the claims. Further, one of skill in the art would not be motivated to make such a combination. Therefore, the present invention is not obvious in light of any combination of Huang et al and/or Wolf. Withdrawal of the §103 rejections is therefore respectfully requested.

III. Conclusion

In view of the foregoing discussion, Applicants have responded to each and every rejection of the Official Action, and respectfully request that a timely Notice of Allowance be issued. Applicants have clarified the structural distinctions of the present invention. Applicants respectfully submit that the foregoing discussion does not present new issues for consideration and that no new search is necessitated. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. §112 and §103, and further examination of the present application.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

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